REMARKS

The Office Action dated February 1, 2005 has been received and carefully noted. The above amendments to claim 40, and the following remarks, are submitted as a full and complete response thereto.

Applicants thank the Examiner for acknowledging that claims 1-12, 14, 20-23, 25, 31-34, 37-38, and 41-42 are allowed. Applicants also thank the Examiner for acknowledging that claims 19 and 30 contain allowable subject matter.

Claims 1, 14-16, 20, 25-27, 31, 35, 37, and 40-41 are independent claims. Claims 1-12, 14, 20-23, 25, 31-34, 37-38, and 41-42 having been allowed and claims 19 and 30 having been objected to. Claims 15-19, 26-30, 35, and 40 are respectfully submitted for consideration.

Claims 1-12, 14-23, 25-35, 37-38, and 40-42 are pending in the present application.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at pages 2-3, claims 15, 26, and 40 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,157,643 to Ma ("Ma"). The Office Action took the position that although Ma does not teach or suggest "wherein said predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks," as recited in independent claims 15 and 26, and "storing the packet in a memory in accordance with a predetermined

algorithm," as recited in independent claim 40, it would have been obvious to arrive to the claimed recitations as a matter of design choice. The rejection is traversed and reconsideration is requested.

Claim 15 recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch buildings blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data. The at least one of the predetermined number of switch building blocks also includes a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. Also, the predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks.

Claim 16 recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data. The at least one of the predetermined number of switch building blocks also includes a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. Also, the at least one data port interface includes at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a

first data rate and at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

Claim 40 recites a method of handling packets in a network switch. The method includes the steps of receiving a packet in a clustered network switch, determining a destination address of the packet from a lookup operation in a common table, and forwarding the packet to the destination address determined from the lookup operation. The receiving step further includes the steps of receiving a packet on at least one of a data port interface and a stack link interface and storing the packet in a memory in accordance with a predetermined algorithm by allocating memory locations between an internal memory and an external memory based upon an amount of internal memory available for an egress port of the clustered network switch from which the packet is to be transmitted.

As will be discussed below, Ma fails to disclose or suggest all of the elements of any of the presently pending claims.

Fig. 2 of Man provides a Clos network having both the first and third stage comprised of k switch elements. See column 5, lines 46-50. Man specifically indicates that a number of alternative paths between switch input i and output j is equal to a number of internal stage switch elements. See column 6, lines 17-20. In addition, in Fig. 4 and column 7, line 57, to column 8, line 9, Man illustrates and describes a switch configuration, where an input stage of a switch is divided into two successive parts, the first of which is formed by the routing network RNW and the second by the shift network

SNW. The routing network comprises k mutually identical routing network elements RE, (i=0, 1, . . . , (k-1)), each having n inputs and n outputs.

In addition, the shift network in Man comprises k mutually identical transfer network elements SHE, (i=0, 1, . . . , (k-1)), each also having n inputs and n outputs. Output j of element RE_i is connected to input j of element SHE_i. Thus, such a combined routing/shift network makes it possible to distribute cells, which are destined for the same switch element of the output stage, over different switch elements in the internal switch stage. Thus, as clearly described in Man, in order to reduce internal blocking, the number of routing network elements and shift network elements, which are connected in series, is equal to the number of switch elements. See Fig. 4 of Man. Man does not teach or suggest that the number of routing network elements and shift network elements is one less than the number switch elements. As a result, Man fails to teach or suggest, "wherein said predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks," as recited in independent claims 15 and 26.

As discussed in the Specification of the present application, one of the many advantages of the claimed invention is that it provides numerous options for combination of port speeds and logical port connectivities.

The Office Action correctly recognized that Man fails to teach or suggest, "wherein said predetermined number of stack link interfaces is configured to be one less than the predetermined number of switch building blocks," as recited in independent

claims 15 and 26. Accordingly, to arrive to the claimed recitation, the Office Action conclusively provides "since this is a design option for one of ordinary skill in the art to decrease the stack interfaces by any number. This feature is obvious as a matter of design choice..." However, there is no teaching or suggestion in Man of modifying the number of routing network elements and shift network elements to be one less than the number of switch elements as recited in independent claims 15 and 26.

To set forth a prima facie obviousness case, evidenced motivation must be provided indicating why one skilled in the art would be motivated, lead, or suggested to modify an existing reference in view of another reference. In addition, is also improper to base a rejection on the claimed feature being merely a design choice. See In re Garrett, 1986 Pat. App. LEXIS 8 (Bd. Pat. App. 1986), where the U.S. Patent and Trademark Office Board of Patent Appeals and Interferences ("Board") specifically stated: "the examiner has not presented any line of reasoning as to why the artisan would have been motivated to so modify the...structure, and we know of none. The examiner's assertion...that the proposed modification would have been "an obvious matter of engineering design choice well within the level of skill of one of ordinary skill in the art" is a conclusion, rather than a reason." Similar discussions can be seen in In re Chu, 36 USPQ2d 1089 (Fed. Cir. 1985).

If the U.S. Patent and Trademark Office wishes to take Official Notice that the proposed functional modification is notoriously well known, Applicants respectfully

request to the Examiner that supporting evidence be provided, such as a reference or an Affidavit signed by the Examiner of record.

In view of the arguments presented above, it is respectfully asserted that Man fails to teach or suggest all the recitations of independent claims 15 and 26, and, accordingly, the obviousness rejection should be withdrawn.

Referring to independent claim 40, this claim recites, "storing the packet in a memory in accordance with a predetermined algorithm." The Office Action has recognized that Ma fails to teach or suggest that the packet is stored in accordance with an algorithm. The Office Action then proceeds to assert that because Ma does teach using buffers to receive packets, "it would have been obvious to one of ordinary skill in the art that an algorithm must be used to control the storage of packets in the buffers." However, it is not proper to arrive to the recitations of independent claim 40 without a showing of a teaching or suggestion in the cited reference that an algorithm may be applied to the buffers to store packets.

To further clarify the present invention, independent claim 40 has been amended further defining the predetermined algorithm. Although Ma generally describes a buffer, the cited reference does not teach or suggest that a predetermined algorithm may be used to store the packets in the buffer by "by allocating memory locations between an internal memory and an external memory based upon an amount of internal memory available for an egress port of the clustered network switch from which the packet is to be

transmitted," as recited in independent claim 40. Accordingly, it is respectfully requested that independent claim 40 be allowed.

In the Office Action, at pages 2-3, claims 16-18, 20, 27-29, and 31 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,625,121 to Lau et al. ("Lau") in view of U.S. Patent No. 6,226,292 to DiPlacido ("DiPlacido"). The Office Action took the position that a combination of Lau and DiPlacido describes the recitations of independent claims 16, 20, 27, and 31. The rejection is traversed and reconsideration is requested.

Claim 16, upon which claim 17-18 depend, recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. At least one of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data and a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. The at least one data port interface also includes at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate and at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate.

Claim 20 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a

meshed configuration. At least one of the predetermined number of switch building blocks comprises at least one data port interface supporting a plurality of data ports for transmitting and receiving data. A predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. Each of the predetermined number of stack link interfaces further comprise a gigabit stack link interface configured to transmit and receive data from another gigabit stack link interface on another switch building block.

Claim 27, upon which claims 28-29 depend, recites a scalable network switch that includes a predetermined number of switch building blocks interconnected in a meshed configuration. Each of the predetermined number of switch building blocks includes at least one data port interface supporting a plurality of data ports for transmitting and receiving data and a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. The at least one data port interface also includes at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate and at least one second data interface supporting at least one second data port transmitting and receiving data at a second rate.

Claim 40 recites a method of handling packets in a network switch. The method includes the steps of receiving a packet in a clustered network switch, determining a destination address of the packet from a lookup operation in a common table, and

forwarding the packet to the destination address determined from the lookup operation. The receiving step further includes the steps of receiving a packet on at least one of a data port interface and a stack link interface and storing the packet in a memory in accordance with a predetermined algorithm by allocating memory locations between an internal memory and an external memory based upon an amount of internal memory available for an egress port of the clustered network switch from which the packet is to be transmitted.

As will be discussed below, Lau and DiPlacido fail to disclose or suggest all of the elements of any of the presently pending claims.

According to the Office Action, the stack link interface of independent claims 16, 20, and 27 is structurally same as the line cards LC1...LC14 of Lau and the building blocks of independent claims 16, 20, 27, and 31 are structurally same as the switching fabric 12 including switching units SF1...SF16 of Lau. Lau generally provides that each of the sixteen switching units (SF1-SF16) of the switching fabric 12 independently switching one cell from an ingress port (VOQ1-VOQ14,MCQ) of one of the line cards to one or more egress ports (EQ) of the line cards during a time interval called a connection cycle. See column 3, lines 28-32.

However, contrary to the assertions made in the Office Action, in view of the description provided in Lau, this reference does not teach or suggest, "a predetermined number of stack link interfaces configured to transmit data between one of said predetermined number of building blocks and another of said predetermined number of building blocks," as recited in independent claims 16, 20, 27, and 31.

Specifically, the switching unit SF1 (i.e., the building block of independent claims 16, 20, 27, and 31 according to Office Action) is the one element that performs a switching of one cell from an ingress to an egress of the ports of the line cards LCs (i.e., the stack link interface of independent claims 16, 20, 27, and 31 according to Office Action). However, the line cards LC are not configured to transmit data between one of said predetermined number of switching units to another of said predetermined number of switching units. The switching fabric 12 is the element that independently switches the transmission of the data. In addition, the switching units are not stack link interfaces.

In addition, Lau is silent as to teaching or suggesting, "at least one first data port interface supporting a plurality of first data ports transmitting and receiving data at a first data rate; and at least one second data port interface supporting at least one second data port transmitting and receiving data at a second rate," as recited in independent claims 16 and 27. Lau does not contemplate that the ports in the ingress and egress may have first and second rates; rather, Lau is specific to providing a constant bit rate traffic (CBR), such as voice and video. See column 4, lines 35-38.

Although Lau provides that the switch 10 may be a frame relay switch for switching frame relay frames and although the frame relay could be implemented to include first and second rates in view of the recitations provided in independent claims 16 and 27, Lau does not provide that the frame relay switch may be used to include first and second rates for at least two reasons. First, Lau is specifically describes a constant bit rate traffic and, therefore, does not consider variable data rates. Second, Lau indicates that the switch 10 may be a frame relay

switch to be able to switch the transmission, not the rate, of the data between the ingress ports and the egress ports. Thus, the motivation provided in the Office Action to include a frame relay switch to provide variable rates is improper.

The only way a person of ordinary skill in the art would include a frame relay in Lau to vary the data rates is in view of the recitations of independent claims 16 and 27. Only the present invention sets forth all the claimed features, as well as the motivation for combining the same. The outstanding rejection would appear to have taken this teaching of the present invention and applied the same to generate a combination of Lau and DiPlacido, as set forth in the Office Action, to disclose the presently claimed invention. Applicants respectfully assert that the prima facie burden has not been met.

In view of the foregoing, Applicants respectfully submit that modifying Lau to include the fast Ethernet and Gigabit Ethernet links as described in DiPlacido would render the apparatus and method to reduce congestion in a network switching node of Lau, at best, unsatisfactory for its intended purpose and, at worst, completely inoperable. Because such modification is prohibited under MPEP § 2143.01, Applicants respectfully request that the rejections to independent claims 16, 20, 27, and 31, and related dependent claims be withdrawn.

In the Office Action, at page 7, claim 35 was rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,625,121 to Lau et al. ("Lau") in view of U.S. Patent No. 6,195,334 to Kadambi ("Kadambi"). The Office Action took the position that a combination of Lau and Kadambi describes the recitations of independent claim 35. The rejection is traversed and reconsideration is requested.

Independent claim 35 recites a scalable network switch, the scalable network switch comprising a predetermined number of switch building blocks interconnected in a meshed configuration. Each of the predetermined number of switch building blocks comprises at least one data port interface supporting a plurality of data ports for transmitting and receiving data. Also, each predetermined number of switch building blocks comprises a predetermined number of stack link interfaces configured to transmit data between one of the predetermined number of building blocks and another of the predetermined number of building blocks. The scalable network switch further comprises a physical layer transceiver in connection with at least one of said plurality of data ports.

As will be discussed below, Lau and Kadambi fail to disclose or suggest all of the elements of any of the presently pending claims.

Regarding the features of independent claim 35 reciting, "a predetermined number of stack link interfaces configured to transmit data between one of said predetermined number of building blocks and another of said predetermined number of building blocks, said scalable network switch further comprising a physical layer transceiver in connection with at least one of said plurality of data ports," this feature was rejected in view of Lau. The arguments presented above supporting the patentability of this claim feature in view of Lau are incorporated herein.

On page 7 of the Office Action, it appears that the description provided in Lau is used to reject the recitations of the predetermined number of stack link interfaces.

However, the Office Action proceeds to assert that "what Ma fails to teach is....It would have been obvious to one of ordinary skill in the art to combine Kadambi with Ma for the purpose of enabling the switch in Ma to transmit and receive data at the physical layer." It appears that this assertion is based on a rejection presented in a previous Office Action. For purposes of advancing prosecution, the combination of Lau and Kadambi will be discussed.

Kadambi generally describes a network switch in a packet switched network having multiple network ports, each having a physical layer transceiver. However, it is respectfully asserted that it is improper to combine Lau and Kadambi. Applicants respectfully submit that the switching fabric disclosed in Lau is designed specifically to reduce congestion in a network switching node. Applicants also respectfully submit that Kadambi is specifically designed to accommodate the use of packets that are not of a constant length. Therefore, Applicants further submit that the suggestion or motivation to combine Lau and Kadambi necessary to establish a prima facie case of obviousness, as discussed in MPEP § 2143, is not present in this instance. At least in view of the above, Applicants respectfully submit that the combination of Lau and Kadambi is improper and that a prima facie case of obviousness has not been properly established against claim 35 of the present application.

At least for the above reasons, Applicants respectfully submit that claim 35 is patentable over Lau and Kadambi, taken either individually or in combination.

Therefore, reconsideration and withdrawal of the rejection of claim 35 under 35 U.S.C. § 103(a) over Lau in view of Kadambi is respectfully requested.

CONCLUSION:

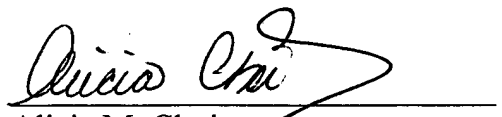
In view of the above, Applicants respectfully submit that the claimed invention recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicants further submit that the subject matter is more than sufficient to render the claimed invention unobvious to a person of skill in the art. Applicants therefore respectfully request that each of claims 15-20, 26-35, and 40 be found allowable and, along with allowed claims 1-12, 14, 21-23, 25, 32-34, 37-38, and 41-42, this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicants respectfully petition for an appropriate extension of time.

Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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